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A Brief History of Software Defined Radio

SDR has come a long way in a short time. Steve Ireland VK6VZ/G3ZZD tells how it became a mainstream technology in amateur radio.

Software Defined Radio (SDR), as it has been carried out by radio amateurs since we started experimenting with it in the early 2000s, is when our receiver uses computer technology to digitally recover the intelligence from a transmitted signal and the corresponding modulation of our transmitter is defined and carried out digitally by computer technology.

Carrying out the recovery process of the signal by computer technology, in the digital rather than the analogue domain, allows us to manipulate and display the signal in a highly-controlled manner using software running on the computer. The signals can be seen in 3D – in their frequency, amplitude and time dimensions, **Fig. 1**.

The first amateur SDRs received signals in a conventional manner via an antenna coupled to a bandpass filter. However, rather than then being fed into an analogue detector/mixer, the wanted signal was sampled using a device called a quadrature sampling detector (QSD). It was then fed into an analogue-to-digital converter (ADC), provided by the soundcard of a personal computer, and digitally processed for display and audio purposes by application software running on the personal computer, **Fig. 2**.

The soundcard, the personal computer and software could also be used for analogue-to-digital conversion in reverse fashion to generate a transmitted signal.

Early examples of radios using this kind of technology are the ready-made, ground-breaking FlexRadio Systems SDR-1000 transceiver (2003) [1] designed by **Gerald Youngblood K5SDR** and its associated open systems PowerSDR application software, and the far cheaper but still well-performing **Tony Parks KB9YIG** Softrock kits (2005) [2] and companion software such as

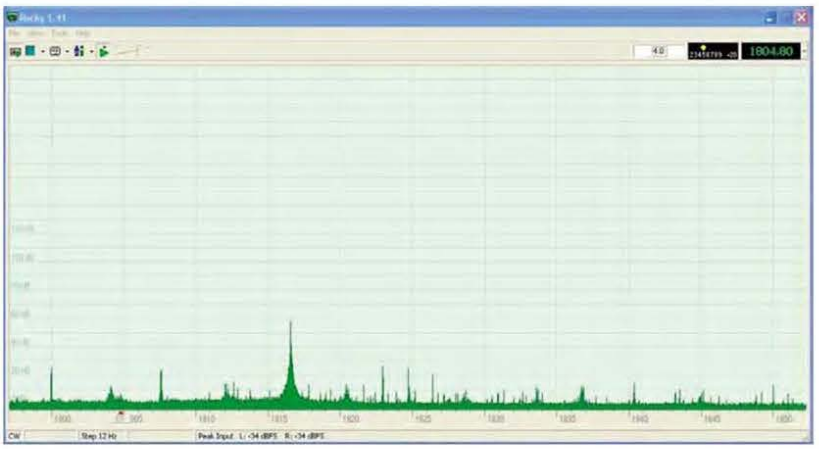

Fig. 1: Signals being shown in frequency, amplitude and time dimensions using VE3NEA's ground-breaking Rocky software.

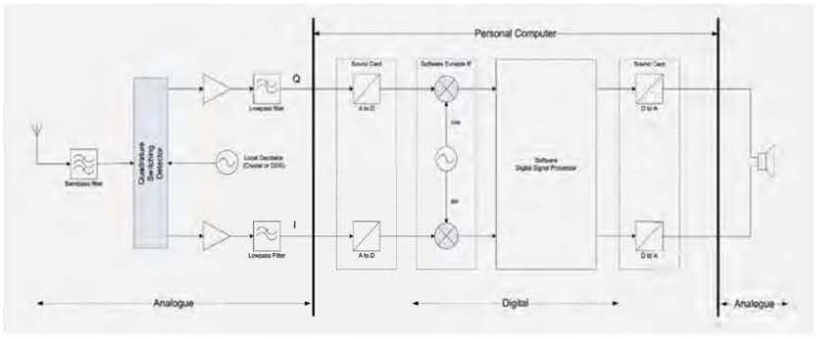

Fig. 2: SDR reception using a quadrature switching detector (QSD).

Alex Shovkoplyas VE3NEA's Rocky [3]. A Softrock V6 receiver is shown in **Fig. 3**.

The receive side of these QSD SDRs can be thought of as a very high performance direct-conversion (DC) receivers, where the sampling detector of the SDR takes the place of the mixer of the DC receiver [4].

A DC receiver mixer produces both the signal and its image (the unwanted sideband of the signal) but the SDR-1000 and the Softrock use their associated software running on a personal computer to balance the phase and amplitude of the in-phase (I) and quadrature (Q – 90° out of phase) components of the signals from the sampling detector so image rejection is carried out and automatically maximised.

This technology or sampling architecture forms the basis of the Elecraft KX3 (2011), which effectively has its own internal computer technology and associated software to carry out the control of the sampling detector, image rejection and analogue-to-digital conversion.

Whereas the average DC receiver can only manage about 30dB image rejection, the automatic image rejection in the Softrock/Rocky combination and the more modern Elecraft KX3 can achieve up to 90dB!

The QSD SDR hardware was quickly developed in both the ready-made (such as FlexRadio 3000/5000 series) and kit (Softrock RXTX, **Fig. 4**) markets, in parallel with the development of rapidly improved functionality in the associated software (as in PowerSDR and Rocky 3.0, which introduced a CW transmit mode). However, as this progress was being made, the SDR world was about to take a quantum leap…

Quantum Leap Time

In 2007, fast (16-bit) ADC integrated circuits became widely available at reasonable prices – specifically, the Linear Technology LTC-2208 chip at around US $100. This sparked the development of the second generation of SDRs because the LTC-2208 was fast enough to allow digital-down-conversion (DDC) and directly convert the zero to 50MHz radio spectrum from analogue to digital at the antenna socket – the 'holy grail' of HF SDR.

The signals could then be digitally processed and converted back to analogue using digital-to-analogue conversion (DAC) circuitry for audio amplification purposes.

Until the emergence of this new generation of ADCs, those available either had too low a dynamic range (they could not deal adequately with both small and large signals) or were too expensive for amateur use, or both.

The LTC-2208 is a saturating ADC that performs in a linear manner until it reaches its overload point. Even after this point, increasing its input level does not produce a catastrophic degradation in performance.

As the result of the LTC-2208 introduction, the open High Performance Software Defined Radio (openHPSDR) group [5] was formed by experimenters such as **Bob McGwier N4HY**, **Phil Covington N8VB**, **Bill Tracey KD5TFD** and my great friend and regular co-writer, **Phil VK6PH** (formerly **VK6APH** and originally **G3WXO**) with the aim of producing a quality DDC receiver – see **Fig. 5**, which shows this architecture – and a companion Digital-Up-Conversion (DUC) transmitter.

There were several key design challenges for the openHPSDR group, the first of which was, ironically, the LTC-2208's remarkable ability to simultaneously convert zero to 60+MHz from analogue to digital. This

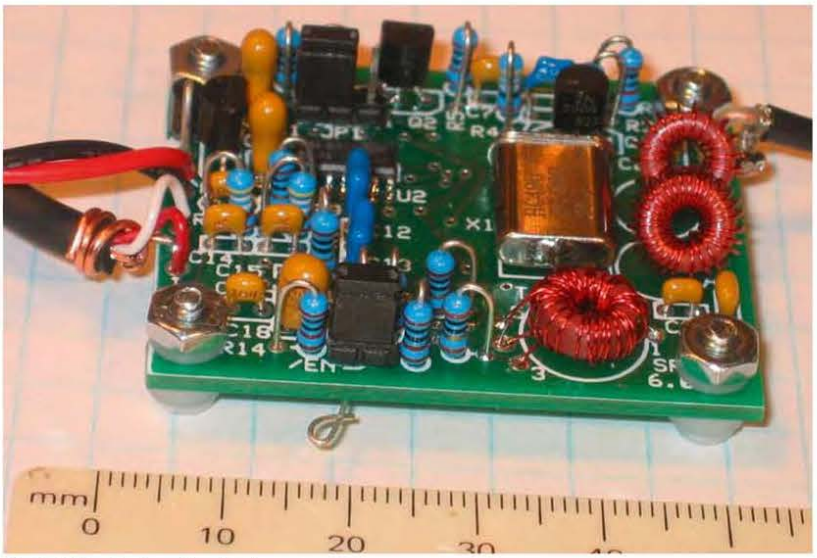

Fig. 3: Softrock v6 receiver hardware.

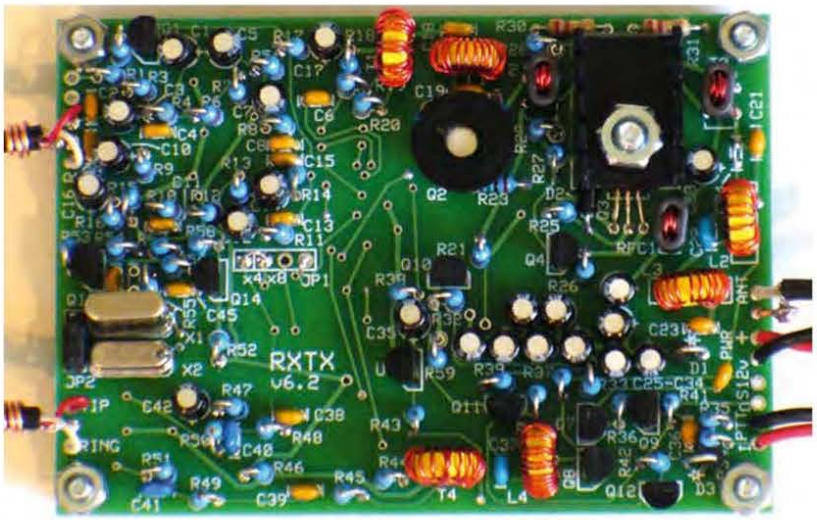

Fig. 4: Softrock RXTX transceiver hardware.

meant that there had to be a digital signal processor after the ADC capable of 'drinking' this ocean of data. Not surprisingly, this feat was beyond the capabilities of any personal computer or device affordable by a radio amateur at that time!

The 16-bit LTC 2208 ADC, **Fig. 6**, samples analogue signals at the rate of approximately 130 mega samples per second (Msps), so the data output stream would be 16 x 130MSPS – over two gigabytes per second!

Luckily some basic analogue radio principles came to the rescue. In a superhet receiver the mixer is followed by a narrowband filter, such as a crystal or capacitor-inductor based type, whose job is to prevent high signal levels on either side of our wanted signal from overloading the receiver. In this case digital filtering is used to cut down the data speed, using a technique called decimation. This technique means sampling only one thousandth of the data after the ADC and throwing the other 999 samples away!

Now if decimation is carried out by a factor of three, this drops the output data rate of an ADC by one-third – in the case of an LTC-2208 to just over 43.3Msps. However, this also means that the maximum input frequency that can be used also drops by (over) a third – in the LTC-2208 to around 10MHz.

To beat the 10MHz maximum, the openHPSDR group used another superhet concept – frequency conversion – where a local oscillator is mixed with the signal

frequency to produce a lower frequency output that can be coped with by the ADC. Instead of a conventional analogue oscillator, a digital Numerically-Controlled-Oscillator (NCO) is used. **Fig. 7** shows the similarities between a superhet and a DDC receiver.

To fully implement the DDC process – carry-out decimation, provide some sophisticated digital filtering required before decimation and create the NCO – there was a need for a digital device that had lots of logic gates that could be programmed to carry out these functions, some in parallel. Enter the Field Programmable Gate Array (FPGA).

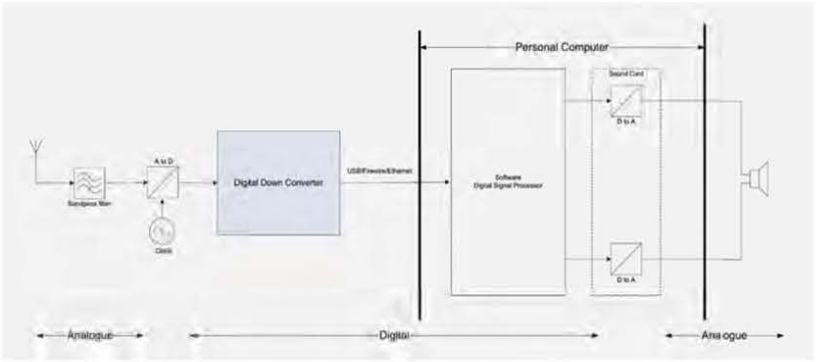

Fig. 5: SDR reception using digital down conversion (DDC).

The FPGA

An FPGA is a 'chip' whose many, many gates can be configured and linked by downloading software code into it. Rather than in the bad old days when a programmer had to access individual gates, a configured FPGA holds a number of specific configurations of gates (known as Logic Elements). A large FPGA may contain well over a million!

While the ADC carries out the actual digital down conversion, it is the FPGA that does the 'heavy lifting' in a DDC design [6].

The openHPSDR group developed the first DDC/DUC SDR transceiver (entirely open-source in terms of its software/hardware) in modular form in the mid-2000s. The original basic modules – Mercury receiver, Penelope transmitter, Ozymandias USB interface and LPU power supply mounted on the Atlas backplane. Later, openHPSDR boards such as the Pennywhistle 20W power amplifier and Alexaires ('Alex') transmit and receive filters did not use the Atlas bus.

By then the open systems PowerSDR software, which was originally developed for the FlexRadio SDR-1000, had split into two versions. One was being developed internally by FlexRadio for its growing product line of QSD-based transceivers (Flex 3000 and 5000 series). The other was developed by the openHPSDR group, in particular **Bill KD5TFD** and **Doug Wigley W5WC**, and continued with the open systems philosophy of software development that FlexRadio founder Gerald Youngblood K5SDR had originally established.

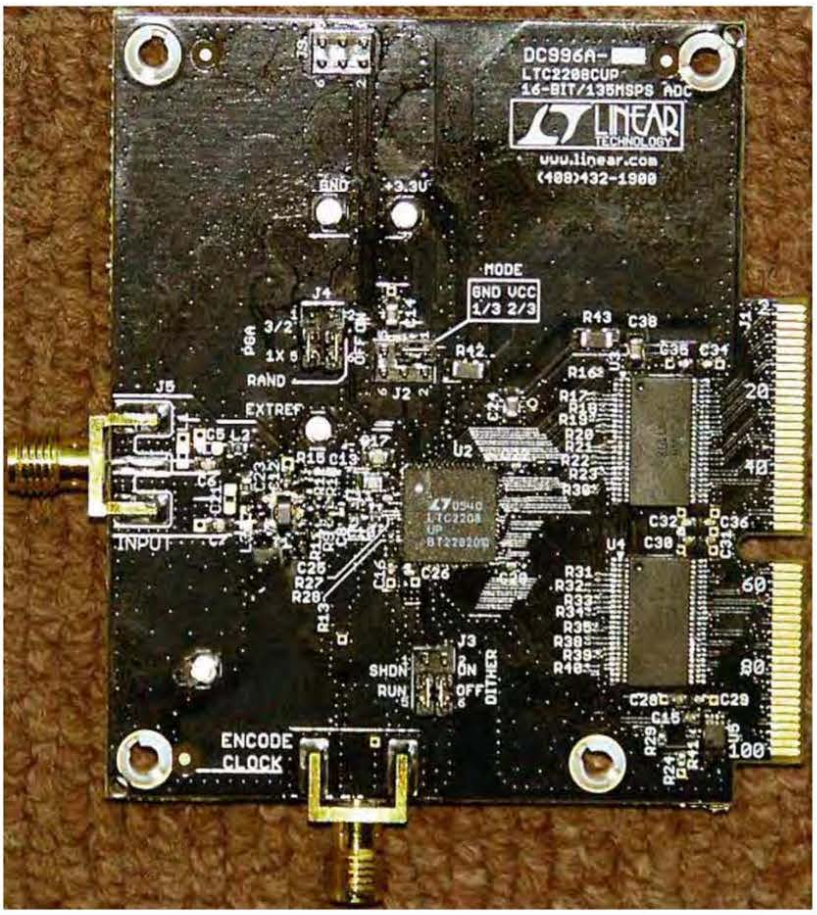

Fig. 6: LTC2208 ADC evaluation hardware.

Bandscope

At the same time, those experimentally-minded radio amateurs who were interested in the bandscope feature that SDR could deliver, in particular the ability to 'point and click' on a station displayed on the bandscope and have their transceiver automatically tune to this frequency, were adding this feature to their existing analogue HF transceivers.

To do this, a small QSD SDR such as a Softrock with suitable frequency coverage was tapped into one of the intermediate frequency (IF) chains of a transceiver such as a Yaesu FT-1000, FT-1000MP or Kenwood TS-570D. In my case, using an FT-1000, VK6PH and KB9YIG helped me with retuning a Softrock V6 receiver to around 8.215MHz to match the FT-1000 second IF and its output was displayed in the Rocky software running on my PC, after analogue to digital conversion by an M-Audio D44 soundcard [7].

The inventor of this method was Alex VE3NEA, who had done this with his own Kenwood TS-570D. Rocky was Alex's first effort in making bandscope software and part of what was to become CW Skimmer (2007), which for a CW operator offered a bandscope/multi-channel CW decoder and

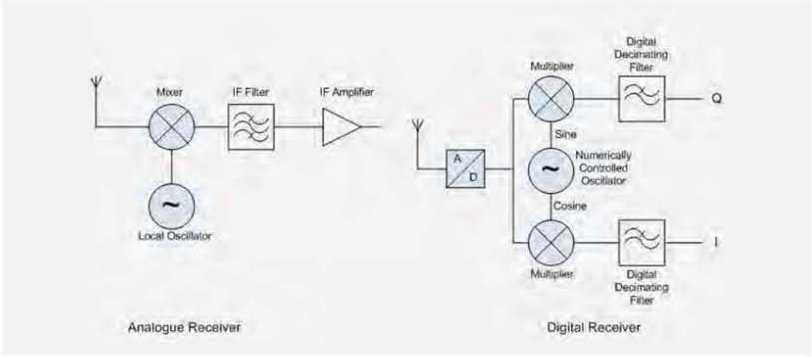

Fig. 7: Comparison between architecture of (left) analogue superheterodyne receiver and (right) DDC

Fig. 8: VK6PH openHPSDR station in 2008, with main boards (left) and Alexaires transmit/receive filtering (right).

analyser program that is still without peer today.

For the following several years, two streams of SDR development evolved in amateur radio – SDR receivers (predominantly QSD in design), which gave bandscope and computer-control facilities to existing superheterodyne transceivers, and the design of DDC and DUC architecture transceivers that could be built by experimenters.

One of the other major issues that the openHPSDR group faced aside from the complexity of FPGA coding was the production of the necessary DDC/DUC hardware. While the design of the circuitry and associated PCBs were something the group members thought they could carry out themselves, the level of expertise needed in the construction of the boards, which used the latest Surface Mount Device (SMD) components, was beyond the abilities of most radio amateurs.

While prototypes could be built using microscopes (with considerable difficulty), what was needed was someone who could construct the boards. As a result, Phil VK6PH and the openHPSDR group approached the Tucson Amateur Packet Radio Group (TAPR) who agreed to produce the boards in 2009. One of the TAPR members was **Scotty Cowling WA2DFI**, whose daytime job was running a PCB manufacturing company, which made the HPSDSR boards, **Fig. 8**, to be offered for sale by TAPR over the internet.

At the time, I had a 'bet each way' and assembled a basic openHPSDR, **Fig. 9**, with the assistance of VK6PH but continued to use a Softrock receiver plugged into the IF of my newly-acquired (and recently launched) Elecraft K3, so as to provide bandscope and control facilities using CW Skimmer. Fortunately, Elecraft had realised the way radio amateurs wanted to operate had changed and designed the K3 with a dedicated IF output (8.215 MHz), allowing the easy use of an SDR-based bandscope.

The K3 was followed by Elecraft's own P3 stand-alone bandscope (which appears to be a DDC SDR) plus several external IF-compatible SDR receivers, such as the LP-Pan. Also new to the market were SDR USB dongles such as the FUNcube, which could either be plugged into your personal computer and used as a stand-alone radio or as the basis for an IF-tap bandscope.

Hermes

Meanwhile, the demand for openHPSDR boards was such that the openHPSDR group, led on this occasion by **Kevin Wheatley M0KHZ**, decided to design a small DDC/DUC transceiver that combined the Mercury receiver, Penelope transceiver and Atlas backplane on one Eurocard PCB. The transceiver, called Hermes, used one large FPGA, which merged the Verilog (programming language) FPGA code from both Mercury and Penelope, and had PC connectivity via Ethernet. As in the case of the original openHPSDR, Hermes, **Fig. 10**, was based on an open source model (Open Hardware Licence/Non-Commercial Licence hardware and General Public Licence software).

The Hermes transceiver, covering 50kHz to 55MHz with a 500mW output, was once again produced and sold by TAPR and went on sale in mid-2012 at a cost of US$895 to members and US$940 to non-members – substantially less than the cost of the original openHPSDR boards and at little more than the manufacturing cost.

As interest in Hermes grew, several companies started to manufacture the openHPSDR boards, including iQLabs.com (involving Scotty WA2DFI) in the USA, NT-Electronics in Germany and Apache Labs in India.

In 2012, FlexRadio Systems, which had successfully continued to develop QSD architecture hardware and grown into the first large-scale amateur radio manufacturer selling SDRs, made its long-awaited move into DDC/DUC with its closed architecture SmartSDR software and associated 6000 series hardware.

From the group of those companies selling openHPSDR hardware, Apache Labs, founded by **Abhi Arunoday Prakash**, emerged as the most successful, with their range of ANAN hardware based upon the Hermes architecture. From 2012 FlexRadio and Apache Labs competed strongly against each other, as Flex continued to develop SmartSDR and the openHPSDR group added some new members who helped take openPowerSDR software development to

new heights.

The new openHPSDR software developers included **Warren Pratt NR0V** (who developed a digital pre-distortion algorithm called Pure Signal to drastically improve the intermodulation performance of SSB produced in openHPSDR), **Doug Wigley W5WC** and **Joe Martin K5SO**.

For almost a decade, radio amateurs with a strong technological interest had waited for mainstream amateur radio manufacturers to produce a DDC/DUC SDR transceiver. Although the DSP technology used in radios built by Yaesu, Kenwood, Icom, Ten-Tec and Elecraft had got closer and closer to this goal, the underlying architecture remained superhet. Then, just when it seemed this was never going to happen, Icom launched the IC-7300 in March 2016 – a true self-contained DDC/DUC transceiver with knobs at a price of US$1,499.

Since its launch, over 20,000 IC-7300s have been sold worldwide and SDR has finally reached mainstream acceptance.

Final Thoughts

One of the greatest things about SDR development in amateur radio was that it was entirely initially driven by amateurs – in my opinion particularly by Gerald Youngblood K5SDR, Tony Parks KB9YIG, Alex Shovkoplyas VE3NEA and the evolving membership of the openHPSDR group, of which Phil Harman VK6PH/G3WXO has remained the constant driving force – rather than by longstanding amateur radio manufacturers.

Without them and other pioneering amateurs detailed in this article – and many more of whom there has unfortunately been insufficient space to mention – SDR would have remained a small backwater area of experimentation and we would have been denied the rich and still developing possibilities of radio you can see as well as hear.

References and Notes

[1] A good starting point to find out about the FlexRadio SDR-1000 is:
www.eham.net/reviews/detail/4108

Also see the original four-part article written by Gerald Youngblood K5SDR in the ARRL's *QEX* magazine from July/Aug 2002 to Jan/Feb 2003 – *A Software Defined Radio for the Masses*.

[2] Tony Parks KB9YIG is still selling Softrock kits through his Five Dash business and there is a Yahoo support group – see:
http://fivedash.com

[3] Rocky (now on version 3.8) can be downloaded as freeware from:
www.dxatlas.com/rocky

[4] As shown in Fig. 2, in modern direct-conversion receivers and QSD SDRs, the unwanted image is removed through cancellation by using two mixers instead of one, and a local oscillator which has a quadrature output (two outputs differing phase by 90°).

[5] In reality, the prime purpose of the SDR hardware in DDC radios is to reduce the data rate of the analogue-to-digital conversion to a slower rate such that the associated PC can process it. For a DDC receiver, if we consider the data rate required for, say, digitising the entire HF spectrum from 0 to 30MHz, with 16 bits per sample, then the minimum data rate is:

30 x 2 x 16 = 960 Megabits per second

Note that the factor of two in this formula is because it is necessary to sample at twice the highest received frequency. While the 960 Megabits per second data rate is within the specification of a Gigabit Ethernet interface, the PC needs to process this data at a sustained rate, which VK6PH has said that even for a fast personal computer is like 'drinking from a fire hose'.

[6] In the openHPSDR receiver, the associated FPGA programming was carried out in the Verilog language, requiring many thousands of hours of work by the design team. In my opinion, it is the complexity and sophistication of this FPGA programming that held back the commercial development of DDC/DUC SDRs until recent years. For more details of openHPSDR, see:
www.openHPSDR.org

[7] See page 8.17 in the RSGB's *Radio Communication Handbook* (11th edition).

Fig. 9: VK6VZ openHPSDR station in 2012, using OpenHPSDR mRX software.

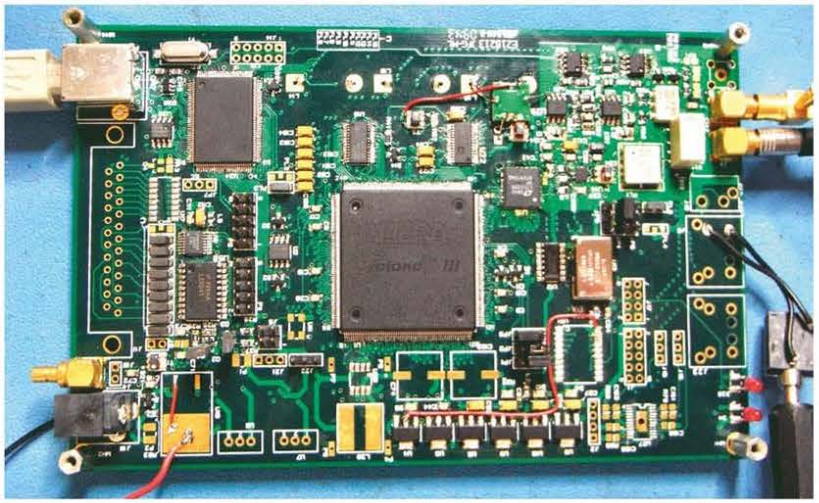

Fig. 10: VK6PH Hermes prototype board.